a display portion in which a plurality of pixels are two-dimensionally arranged at intersecting points of gate lines as many as a plurality of rows and signal lines as many as a plurality of columns which are wired in a matrix shape;

a plurality of driver circuits for applying a signal potential to each pixel in said display portion through the signal lines of said plurality of columns; and

time-divisional switches for time-divisionally sending a signal potential that is outputted from each of said plurality of driver circuits to the signal lines of said plurality of columns,

characterized in that a time-dividing number of said time-divisional switches is equal to 3,

the number of output terminals of each of said plurality of driver circuits is set to a measure of the total number of signal lines of said plurality of columns,

the number of output terminals of each of said plurality of driver circuits is set to a same number,

when a size of a frame portion adjacent to said display portion is specified, the number (n) of output terminals of each of said plurality of driver circuits is determined on the basis of said specified frame size by the number of lines which can be wired into a wiring region of said frame portion,

when the total number of signal lines of said plurality of columns that is decided by a display system is set to N, the

C1 w-5.

number of said driver circuits is set to N/n.

11. (amended) A display according to claim 3, characterized in that a leading waveform and a trailing waveform of a signal output waveform of each of said plurality of driver circuits are symmetrical with respect to a time base.

C2

13. (amended) A display according to claim 3, characterized in that a period of time which is selected by said time-divisional switches is equal to or shorter than 1/3 of a horizontal scanning period.

C3

15. (amended) A display according to claim 3, characterized in that a blanking period which is caused for the period of time, selected by said time-divisional switches is equal to or shorter than (a horizontal scanning period - the period of time selected by the time-divisional switches x 3) / 3.

C4

17. (amended) A display according to claim 3, characterized in that said plurality of driver circuits generate a signal potential so as to correct curves of voltage-transmittance characteristics of R (red), G (green), and G (blue) by diving to said time-divisional switches.

C5

18. (amended) A display according to claim 3, characterized in that in a 1H (H denotes a horizontal scanning period) inversion driving or a 1H common inversion driving, the signal line which is selected first by said time-divisional switches is a line of blue, the signal line which is selected at the second time is a line of green, and the signal line which is selected at the third time is a line of red.

C5 cont.

19. (amended) A display according to claim 3, characterized in that in a dot inversion driving, the signal line which is selected first by said time-divisional switches is a line of red, the signal line which is selected at the second time is a line of green, and the signal line which is selected at the third time is a line of blue.

20. (amended) A display according to claim 3, characterized in that time-division of said time-division switches distribute signals to R (red), G (green), and G (blue) constituting one pixel.

C6

25. (amended) A liquid crystal display comprising:

a display portion, said display portion having a plurality of gate lines, a plurality of signal lines and a plurality of pixels,

a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits, said plurality of driver circuits including at least one general driver circuit and one remainder driver circuit,

each said at least one general driver circuit having a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines,

said remainder driver circuit having a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines,

C6 cont.

the quantity of remainder driver circuit output terminals being defined as (S - (OP * (DC-1))), "S" being the quantity of said plurality of signal lines, "OP" being the quantity of general driver circuit output terminals, and "DC" being the quantity of said plurality of driver circuits,

said quantity of general driver circuit output

terminals being different than said quantity of remainder driver circuit output terminals.

26. (amended) A display according to claim 25, wherein each driver circuit of said plurality of driver circuits is separate and distinct from another driver circuit of said plurality of driver circuits.

27. (amended) A display according to claim 25, wherein said plurality of pixels is arranged in a two-dimensional matrix shape.

37. (amended) A display according to claim 25, wherein an output terminal of said plurality of driver circuits is electrically connected to an input terminal of a time-divisional switch, said time-divisional switch providing a de-multiplexed signal potential to said signal line, said de-multiplexed signal potential being a signal potential for one of a plurality of primary colors that is time-divided from another signal potential for another of said plurality of primary colors and supplied to said signal line.

Please add the following new claims.

43. (new) A display according to claim 37, wherein said plurality of primary colors is a first primary color, a second primary color and a third primary color.

44. (new) A display according to claim 25, wherein said quantity of general driver circuit output terminals is greater than said quantity of remainder driver circuit output terminals.

45. (new) A display according to claim 25, wherein the sum total of general driver circuit output terminals and said remainder driver circuit output terminals is equal to said plurality of signal lines.

C4

46. (new) A display according to claim 25, wherein said plurality of driver circuits include more than one said general driver circuit.

47. (new) A display according to claim 46, wherein each said general driver circuit has an equal number of general driver circuit output terminals.

48. (new) A display according to claim 25, wherein said plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on